Sequential Circuits

Chapter 4

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Outline

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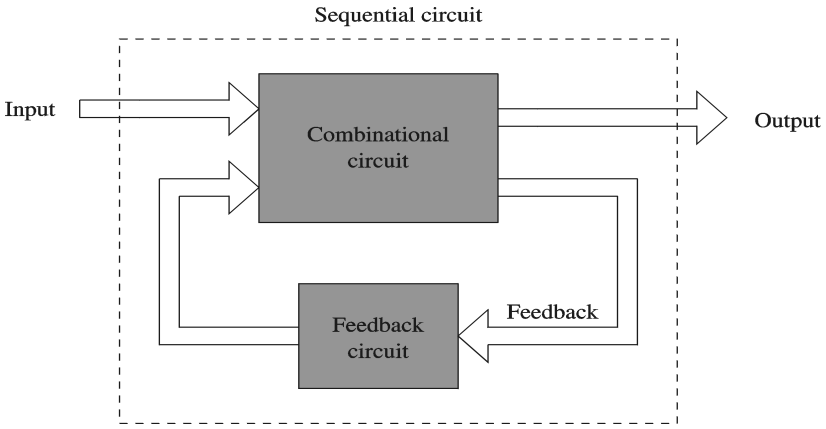
  - Propagation delay
- Latches
  - SR latch
  - Clocked SR latch
  - D latch
  - JK latch
- Flip flops
  - D flip flop
  - JK flip flop
- Example chips
- Example sequential circuits
  - Shift registers
  - Counters
- Sequential circuit design
  - Simple design examples
    - Binary counter
    - General counter
  - General design process
    - Examples
      - Even-parity checker
      - Pattern recognition

Introduction

- Output depends on current as well as past inputs
  - Depends on the history
  - Have "memory" property
- Sequential circuit consists of
    - » Combinational circuit
    - » Feedback circuit
  - Past input is encoded into a set of state variables
    - » Uses feedback (to feed the state variables)
      - – Simple feedback
      - – Uses flip flops

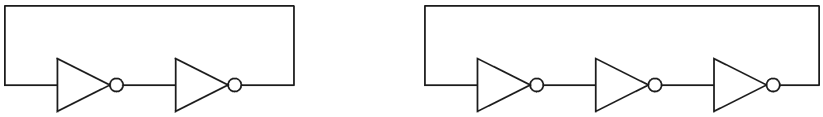
Introduction (cont'd)

Main components of a sequential circuit



Introduction (cont'd)

- Feedback circuit can be
  - A simple interconnection some outputs to input, or
  - A combinational circuit with "memory" property
    - Uses flip-flops we discuss later
- Feedback can potentially introduce instability

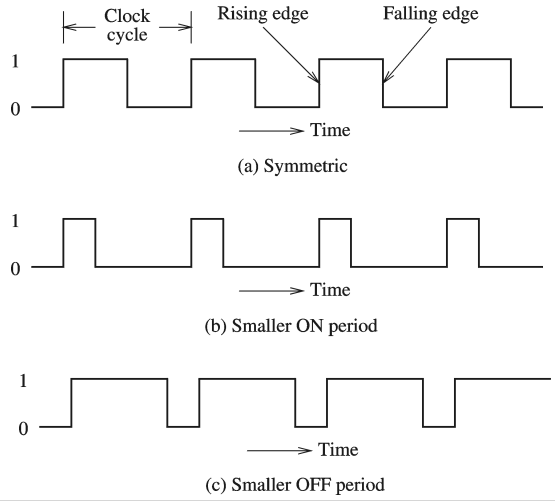


(a) Stable circuit (b) Unstable circuit

Clock Signal

- Digital circuits can be operated in
  - Asynchronous mode
    - Circuits operate independently
      - Several disadvantages
  - Synchronous mode
    - Circuits operate in lock-step
    - A common clock signal drives the circuits
- Clock signal
  - A sequence of 1s and 0s (ON and OFF periods)
  - Need not be symmetric

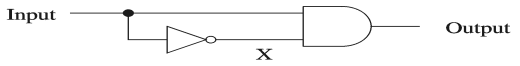
Clock Signal (cont'd)



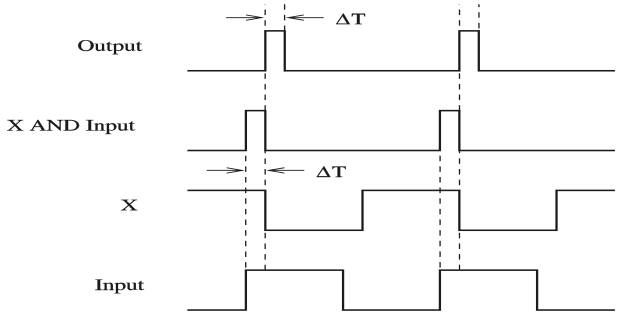
Clock Signal (cont'd)

- Clock serves two distinct purposes
  - Synchronization point
    - Start of a cycle
    - End of a cycle
    - Intermediate point at which the clock signal changes levels
  - Timing information
    - Clock period, ON, and OFF periods
- Propagation delay
  - Time required for the output to react to changes in the inputs

Clock Signal (cont'd)



(a) Circuit diagram

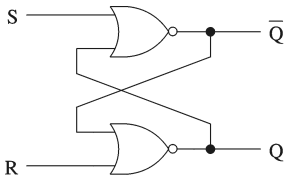


(b) Timing diagram

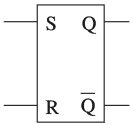
Latches

- Can remember a bit
- Level-sensitive (not edge-sensitive)

A NOR gate implementation of SR latch



(a) Circuit diagram



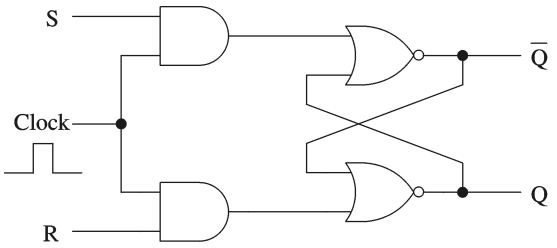
(b) Logic symbol

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	0

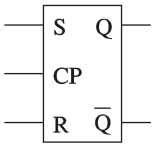
(c) Truth table

Latches (cont'd)

- SR latch outputs follow inputs
- In clocked SR latch, outputs respond at specific instances
  - Uses a clock signal



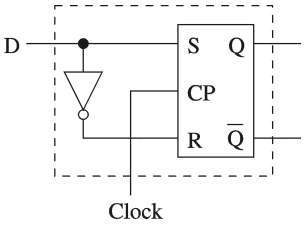
(a) Circuit diagram



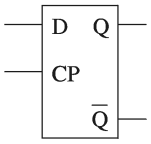
(b) Logic symbol

Latches (cont'd)

- D Latch
  - Avoids the SR = 11 state



(a) Circuit diagram



(b) Logic symbol

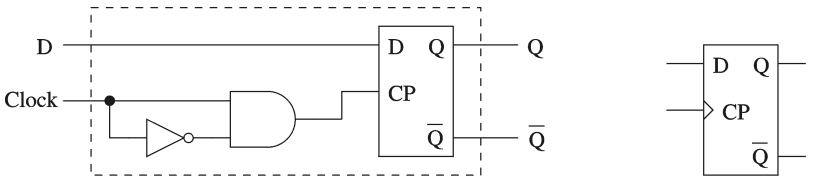
D	Q_{n+1}
0	0
1	1

(c) Truth table

Flip-Flops

- Edge-sensitive devices
  - Changes occur either at positive or negative edges

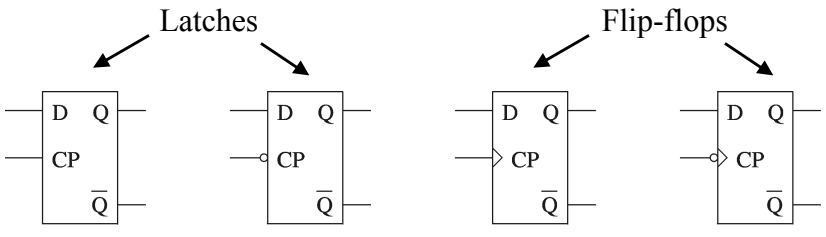
Positive edge-triggered D flip-flop



(a) Circuit diagram (b) Logic symbol

Flip-Flops (cont'd)

- Notation
  - Not strictly followed in the literature
    - » We follow the following notation for latches and flip-flops



(a) (b) (c) (d)

Low level High level Positive edge Negative edge

Flip-Flops (cont'd)

JK flip-flop
(master-slave)

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$